

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,068,672 B1
APPLICATION NO. : 09/874395
DATED : June 27, 2006
INVENTOR(S) : James W. Jones

Page 1 of 4

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

(56) References Cited

Please insert the following U.S. PATENT DOCUMENTS:

5,119,367	06-1992	Kawakatsu et al.
5,295,135	03-1994	Kammerl, Anton
5,365,521	11-1994	Ohnishi et al.
5,455,826	10-1995	Ozveren et al.
5,500,858	03-1996	McKeown
5,577,035	11-1996	Hayter et al.
5,604,867	02-1997	Harwood, Michael J.
5,710,549	10-1998	Horst et al.
5,781,320	07-1998	Byers, Charles Calvin
5,923,644	07-1999	McKeown et al.
5,982,771	11/09/1999	Caldara et al.
5,987,026	11-1999	Holland, Peter
6,014,367	01-2000	Joffe
6,014,431	01-2000	McHale et al.
6,072,800	06-2000	Lee
6,134,217	10-2000	Stiliadis et al.
6,160,812	12-2000	Bauman et al.
6,181,694	01-2001	Pickett, Scott K.
6,195,355	02-2001	Demizu
6,262,986	07-2001	Oba et al.
6,327,253	12-2001	Frink
6,385,678	02-2002	Jacobs et al.
6,389,480	05-2002	Kotzur et al.
6,501,731	12-2002	Chong et al.
6,798,784	09-2004	Dove et al.

Please insert the following OTHER PUBLICATIONS:

PCT/US02/17515 PCT Search Report, dated 12 Dec. 2002, 1 pg;

PCT/US02/17515 Int'l Preliminary Examination Report, dated 12 Nov. 2003, 7 pgs;

Office Action dated September 28, 2004, (US Patent Application 10/199,996) (8 pages);

Response to Amendment dated September 28, 2004, (US Patent Application 10/199,996), filed January 24, 2005, (8 pages);

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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Office Action dated September 28, 2004 in EP Application No. 03254534.5-2416 based on US Patent Application 10/199,996 (5 pages total excluding cover sheet);

Search Report dated October 15, 2003 in EP Application No. 03254534.5-2416 based on US Patent Application 10/199,996 (2 pages total excluding cover sheet);

“The iSLIP scheduling algorithm for input-queued switches,” by N. W. McKeown in IEEE/ACM Transactions on Networking, vol. 7, no. 2, April 1999;

T. Anderson, S. Owicki, J. Saxe and C. Thacker, “High Speed Switch for Local Area Networks”, ACM Transactions on Computer Systems, vol. 11, no. 4, Nov. 1993 pp. 1-13;

N. W. McKeown, M. Izzard, A. Mekkittikul, W. Ellersick and M. Horowitz, “The tiny tera: A packet switch core”, Hot Interconnects V., August 1996, pp. 1-13;

A. Parekh, R. Gallager, “A Generalized Processor Sharing Approach To Flow Control in Integrated Services Networks: The Multiple Node Case”, IEEE/ACM Transaction On Networking, VOL. 2, NO. 2, APRIL 1994, pp. 136-151;

A. Parekh, R. Gallager, “A Generalized Processor Sharing Approach To Flow Control in Integrated Services Networks: The Single Node Case”, IEEE/ACM Transaction On Networking, Vol. 1, No. 2, JUNE 1993, pp. 344-357;

D. Stiliadis, A Varma, “Efficient Fair-Queueing Algorithms for Packet-Switched Networks”, IEE/ACM Transaction On Networking, Vol. 6, No. 2, 1998, Article No. 27473, pp. 1-11 and B.1-B.2;

M. Goureau, S. Kolliopoulos, S. Rao, “Scheduling Algorithms for Input-Queued Switches: Randomized Techniques and Experimental Evaluation”, IEEE/Infocom 2000, pp. 1634-1643;

J. Bennett, Hui Zhang “Why WFQ Is Not Good Enough For Integrated Services Networks”, 1996, pp. 1-8;

N. McKeown, A. Mekkittikul, V. Anantharam, J. Walrand, “Achieving 100% Throughput in an Input-Queued Switch”, IEEE Transaction Communications, Vol. 47, No. 8, August 1999, (22 pages);

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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

I. Stoica, S. Shenker, H. Zhang, "Core-Stateless Fair Queueing: Achieving Approximately Fair Bandwidth Allocations in High Speed Networks",
[Http://www-2.cs.cmu.edu/~istoica/sig98talk/](http://www-2.cs.cmu.edu/~istoica/sig98talk/), 1998, pp1-20;

N. KcKeown, "Scheduling Algorithms for Input-Queued Cell Switches", © 1995,
pp. 1-119;

R. Schoenen, "An Architecture Supporting Quality-of-Service in Virtual-Output-Queued Switches", iEICE Transaction Communications, Vol. E83-B, No. 2,
February 2000, pp. 1-10;

M.J.G. van Uitert, S.C. Borst, "A Reduced-Load Equivalence For Generalized Processor Sharing Networks With Heavy-Tailed Input Flows", Probability, Networks and Algorithms (PNA), PNA-R007, August 31, 2000, pp. 1-37;

N. Joy, K. Jamadagni, "Optimal Call Admission Control in Generalized Processor Sharing (GPS) Schedulers", IEEE Infocom 2001, pp. 1-10;

D. Stiliadis, A. Varma, "Rate-Proportional Servers: A Design Methodology for Fair Queueing Algorithms", UCSC-CRL-95-58, December 1995, pp. 1-22 and A.1-A.4;

D. Staliadis, A. Varma, "Latency-Rate Servers: A General Model for Analysis of Traffic Scheduling Algorithms", IEEE/ACM Transactions of Networking, Vol. 6, No. 5, October 1998, pp. 611-624;

M. Vishnu, "Implementing VirtualClock without Cell Stamps", IEEE Communications Letters, 1997, pp. 1-3;

M. Vishnu, J. Mark, "A Flexible Service Scheduling Scheme for ATM Networks", DBLP Record 'conf/infocom/VishnuM96, pp. 647-654;

M. Vishnu, J. Mark, "Reference Queue Tracking Strategies for Delay Guarantees in ATM Networks", November 4, 1997, pp. 1-22;

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M. Vishnu, J. Mark, "Reference Queue Tracking Strategies for Delay Guarantees in ATM Networks", November 22, 1999, pp. 1-18;

M. Vishnu, J. Mark, "HOL-EDD: A Novel Service Scheduling Scheme for ATM Networks", June 16, 1997, pp. 1-23.

Signed and Sealed this

First Day of April, 2008

A handwritten signature in black ink, appearing to read "Jon W. Dudas". The signature is stylized with a large, looped initial "J" and a cursive "Dudas".

JON W. DUDAS
Director of the United States Patent and Trademark Office